Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application. Please cancel claims 4, 5, 11, 12, 18, 19, 26, 27, 31, and 32. Please amend claims 1, 9, 15, 23, and 28, as follows:

Listing of Claims:

1. (Currently amended) A memory module for a memory system, comprising:

a plurality of memory devices; and

a memory hub, comprising:

a link interface for receiving memory requests for access to at least one of the memory devices, the link interface having transmitter and receiver logic having adjustable timing and voltage levels adjusted according to link interface control signals;

a memory device interface coupled to the memory devices, the memory device interface coupling memory requests to the memory devices for access to at least one of the memory devices, the memory device interface having output buffers having adjustable slew rate and drive strength adjusted according to memory device interface control signals;

a switch for selectively coupling the link interface and the memory device interface; and

a memory hub diagnostic engine coupled to the switch for coupling to the link interface and the memory device interface to perform diagnostic testing of the memory system, the diagnostic engine having a maintenance port to provide access to results of the diagnostic testing and to receive diagnostic testing commands, the memory hub diagnostic engine configured to generate link interface control signals to adjust timing and voltage levels of the link interface and generate memory device interface control signals to adjust slew rate and drive strength of the memory device interface in response to corresponding diagnostic testing commands.

2. (Original) The memory module of claim 1 wherein the memory hub diagnostic engine comprises:

a maintenance port interface to translate diagnostic testing commands into control signals for the memory hub diagnostic engine;

a pattern generator coupled to the maintenance port interface to generate data patterns for the diagnostic testing in response to receiving control signals from the maintenance port interface;

a sequencer coupled to the maintenance port interface to access the memory devices, the sequencer generating memory commands based on the control signals received from the maintenance port interface; and

a switch interface coupled to the maintenance port interface, the pattern generator and the sequencer to provide control signals, pattern data, and memory commands to the switch.

3. (Original) The memory module of claim 1, further comprising a DMA engine coupled to the switch to generate memory commands for the memory devices to execute diagnostic testing.

4. (Cancelled)

5. (Cancelled)

6. (Original) The memory module of claim 1 wherein the maintenance port of the memory hub diagnostic engine comprises a port compatible with a JTAG standard.

7. (Original) The memory module of claim 1 wherein the maintenance port of the memory hub diagnostic engine comprises port compatible with a System Management Bus standard.

8. (Original) The memory module of claim 1 wherein the plurality of memory devices comprises a plurality of synchronous random access memory devices.

9. (Currently amended) A memory hub for a hub-based memory system having a plurality of memory devices, the memory hub comprising:

a link interface for receiving memory requests for access to at least one memory device of the memory system, the link interface having adjustable timing and voltage levels adjusted in accordance with control link interface control signals;

a memory device interface for coupling to the memory devices, the memory device interface coupling memory requests to the memory devices for access to at least one of the memory devices, the memory device interface having output buffers having adjustable slew rate and drive strength adjusted according to memory device interface control signals;

a maintenance bus interface for receiving diagnostic testing commands and translating the same into control signals to perform diagnostic testing of the hub-based memory system, the maintenance bus interface further providing access to results of the diagnostic testing, the maintenance bus interface configured to generate link interface control signals to adjust timing and voltage levels of the link interface and memory device interface control signals to adjust slew rate and drive strength of the memory device interface in response to corresponding diagnostic testing commands;

a pattern generator coupled to the maintenance bus interface to generate data patterns for the diagnostic testing in response to receiving control signals from the maintenance bus interface;

a sequencer coupled to the maintenance bus interface to generate memory commands for accessing the plurality of memory devices based on the control signals received from the maintenance bus interface; and

a link interface and memory device interface controller coupled to the maintenance bus interface, the pattern generator and the sequencer to provide control signals, pattern data, [[and]] memory commands, link interface control signals, and memory device interface control signals to the link and memory device interfaces.

10. (Original) The memory hub of claim 9, further comprising a DMA engine coupled to the link interface, the memory device interface and the maintenance bus interface to generate memory commands for the memory devices of the memory system to execute diagnostic testing in accordance with control signals from the maintenance bus interface.

11. (Cancelled)

12. (Cancelled)

13. (Original) The memory hub of claim 9 wherein the maintenance bus interface comprises a maintenance port compatible with a JTAG standard.

14. (Original) The memory hub of claim 9 wherein the maintenance bus interface comprises a maintenance port compatible with a System Management Bus standard.

15. (Currently amended) A memory system for use in a computer system, the memory system comprising:

a plurality of memory modules, each module comprising:

a plurality of memory devices; and

a memory hub, comprising:

a link interface for receiving memory requests for access to at least one of the memory devices, the link interface having transmitter and receiver logic having adjustable timing and voltage levels adjusted according to link interface control signals;

a memory device interface coupled to the memory devices, the memory device interface coupling memory requests to the memory devices for access to at least one of the memory devices, the memory device interface having output buffers having adjustable slew rate and drive strength adjusted according to memory device interface control signals; and

a switch for selectively coupling the link interface and the memory device interface;

a memory bus to which the memory modules are coupled by the respective link interfaces; and

a memory hub system diagnostic engine coupled to the switches of each module for coupling to the link interface and the memory device interfaces of the memory modules to perform diagnostic testing of the memory system, the diagnostic engine having a maintenance port to provide access to results of the diagnostic testing and to receive diagnostic testing commands, the memory hub system diagnostic engine configured to generate link interface control signals to adjust timing and voltage levels of the link interface and generate memory device interface control signals to adjust slew rate and drive strength of the memory device interface in response to corresponding diagnostic testing commands.

16. (Original) The memory system of claim 15, further comprising a DMA engine coupled to the switches of each module to generate memory commands for the memory devices to execute diagnostic testing.

17. (Original) The memory system of claim 15 wherein the memory hub diagnostic engine comprises:

a maintenance port interface to translate diagnostic testing commands into control signals for the memory hub diagnostic engine;

a pattern generator coupled to the maintenance port interface to generate data patterns for the diagnostic testing in response to receiving control signals from the maintenance port interface;

a sequencer coupled to the maintenance port interface to access the memory devices, the sequencer generating memory commands based on the control signals received from the maintenance port interface; and

a switch interface coupled to the maintenance port interface, the pattern generator and the sequencer to provide control signals, pattern data, and memory commands to the switch.

18. (Cancelled)

19. (Cancelled)

20. (Original) The memory system of claim 15 wherein the maintenance port of the memory hub diagnostic engine comprises a port compatible with a JTAG standard.

21. (Original) The memory system of claim 15 wherein the maintenance port of the memory hub diagnostic engine comprises port compatible with a System Management Bus standard.

22. (Original) The memory system of claim 15 wherein the plurality of memory devices comprises a plurality of synchronous random access memory devices.

23. (Currently amended) A method for performing diagnostic testing on a hub-based memory system having a memory hub, comprising:

coupling diagnostic testing commands to a diagnostic engine located on the memory hub, the diagnostic engine having a maintenance port through which the diagnostic testing commands are coupled;

translating the diagnostic testing commands into control signals;

coupling the control signals from the diagnostic engine to the hub-based memory system to execute diagnostic testing including coupling control signals to link interfaces of the memory hub to monitor the link interfaces and adjust at least one of slew rate and drive strength of the link interfaces; and

monitoring results of the diagnostic testing of the memory system through the maintenance port of the diagnostic engine.

24. (Original) The method of claim 23, further comprising storing the diagnostic testing in a test memory coupled to the diagnostic engine and wherein monitoring results of the diagnostic testing comprises access the test memory through the maintenance port to retrieve the results.

25. (Original) The method of claim 23 wherein coupling the control signals from the diagnostic engine to the hub-based memory system to execute diagnostic testing comprises coupling the control signals to memory controllers of the memory hub to be provided to memory devices of the hub-based memory system.

26. (Cancelled)

27. (Cancelled)

28. (Currently amended) A method for performing diagnostic testing of a hub-based memory system, comprising:

providing diagnostic testing commands to a diagnostic engine located on the memory hub, the diagnostic engine having a maintenance port through which the diagnostic testing commands are coupled;

executing the diagnostic testing including coupling control signals from the diagnostic engine to link interfaces of the memory hub to monitor the link interfaces and adjust at least one of slew rate and drive strength of the link interfaces; and

monitoring results of the diagnostic testing of the memory system through the maintenance port of the diagnostic engine.

29. (Original) The method of claim 28, further comprising storing the diagnostic testing in a test memory coupled to the diagnostic engine and wherein monitoring results of the diagnostic testing comprises access the test memory through the maintenance port to retrieve the results.

30. (Original) The method of claim 28 wherein executing the diagnostic testing comprises coupling control signals from the diagnostic engine to memory controllers of the memory hub to be provided to memory devices of the hub-based memory system.

31. (Cancelled)

32. (Cancelled)